REMARKS

Claims 1-8 are pending in this application, of which claims 1, 2 and 4 have been amended. No new claims have been added.

The Examiner has requested a new, more descriptive title.

Accordingly, the title has been so amended.

Claims 1-3 and 5-7 stand rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent Publication 2002/0127839A1 to Umetsu et al. (hereafter, "**Umetsu et al.**").

Applicants respectfully traverse this rejection.

Umetsu et al. discloses a method of forming a semiconductor device in which a conductive material is provided to an open end of a penetrating hole 24 penetrating through the semiconductor element, on the side of a first surface of the semiconductor element. The conductive material is melted to flow into the penetrating hole. The conductive material is made to flow into the penetrating hole in a state that an atmospheric pressure on the side of a second surface of the semiconductor element opposite to the first surface is lower than an atmospheric pressure on the side of the first surface.

FIG. 2A shows that penetrating hole 24 is formed in an insulating material 22 covering one side of the semiconductor chip, and extends through the semiconductor chip 10 and the conductive pad 14 (and metal covering 16). Conductive material 40 is forced through the penetrating hole 24 so as to provide a rounded conductive surface on opposite sides of the semiconductor device.

The Examiner urges that items 14, 16 correspond to the wiring patterns of the instant application as shown, for example, in FIG. 1H as wiring pattern 32a.

Applicants respectfully disagree. Items 14, 16 in **Umetsu et al.** are merely conductive pads and metal layers provided on the pads to prevent oxidation of the pads, and are not formed on the insulating film in which the semiconductor chip is buried, as in the present invention. **Umetsu et al.** is directed to forming a semiconductor device, and not to a method of making packaging structure for the semiconductor device, to which the claims of the instant application are directed. Item 1 of **Umetsu et al.** is a single semiconductor device including a single semiconductor chip 10. FIG. 4 shows several of the semiconductor devices 1 stacked on top of each other, but does not show the steps of manufacturing an electronic parts packaging structure, as recited in claims 1-3 and 5-7, where the "electronic parts" (corresponding to the semiconductor device 1 of **Umetsu et al.**) are covered by an insulating form, and a via hole is formed in the insulating film to reach the connection terminal of the "electronic parts" (semiconductor device), as recited in claims 1 and 2 of the instant application.

Accordingly, claims 1 and 2 have been amended to recite that the electronic parts are flip-chip connected to a wiring substrate such that the electronic parts are buried in an insulating film.

In amended claim 1, because thin electronic parts (150 μm or less) can be used, a total thickness of the electronic parts packaging structure can be reduced, and such packaging structure can respond to a higher density.

In **Umetsu et al.**, through holes are formed in the semiconductor chip, but the

semiconductor chip is not buried in an insulating film, and the insulating film is not formed on the wiring substrate.

Thus, the 35 U.S.C. § 102(e) rejection should be withdrawn.

Claim 4 stands rejected under 35 U.S.C. § 103(a) as unpatentable over **Umetsu et al.** in view of U.S. Patent 6,363,513 to Furukawa et al. (hereafter, "**Furukawa et al.**").

Applicants respectfully traverse this rejection.

Furukawa et al. discloses a method of manufacturing a semiconductor device in which a via hole having a bottom is formed in a substrate and then a conductor layer is formed at least over a sidewall of the via hole. Thereafter, the substrate is thinned by removing a portion of the substrate opposite another portion of the substrate in which the via hole is formed such that the conductor layer is exposed.

Furukawa et al. has been cited for teaching the use of an electroplating method to form a connection terminal but, like **Umetsu et al.** discussed above, is not directed to a method of manufacturing an electronic parts packaging structure in which the electronic parts are flip-chip connected to a wiring substrate such that the electronic parts are buried in an insulating film, as in the present invention.

Thus, the 35 U.S.C. § 103(a) rejection should be withdrawn.

Claim 8 stands rejected under 35 U.S.C. § 103(a) as unpatentable over **Umetsu et al.**

Applicants respectfully traverse this rejection.

The Examiner has indicated that no criticality has been shown regarding the recited

limitation of 150 micrometers or less for the thickness of the semiconductor chip.

As noted above, **Umetsu et al.** is not directed to a method of manufacturing an electronic parts packaging structure, as recited in claim 1, as amended, from which claim 8 depends.

Thus, the 35 U.S.C. § 103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 1-8, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosure: Substitute Abstract of the Disclosure
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